another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced.

3. (AMENDED) An integrated circuit according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal.

4. (AMENDED) An integrated circuit according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal and by a delay time produced by a delay circuit added to the optional integer times as long as a half period of the data input signal.

5. (AMENDED) A liquid crystal display characterized in that multi-port display data output signals are generated with respect to a data input signal, and points of changing said display data output signals with respect to a time base are set with time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced.

7. (AMENDED) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the

clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal.

8. (AMENDED) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal and by a delay time produced by a delay circuit added to the integer times as long as the half period of the clock input signal or the display data input signal.

a3 cncl.

9. (AMENDED) A driving method of a liquid crystal display characterized in that when red, green and blue color display data composed of plural bits are transferred from a display timing circuit to a TFT drive circuit for driving a TFT liquid crystal panel to display, each transfer is performed with a time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said display data.